AMENDMENTS TO THE SPECIFICATION

Kindly amend paragraph [0017] of the specification as follows:

[0017] A conventional clock phase alignment circuit 16 is illustrated in FIG. 1. An improved circuit, incorporated into the drift compensation system according to the invention, includes additional features illustrated in FIG. 2. These features are an additional output carrying information regarding the number of phase steps the clock management circuit 18 is being run, additional inputs (tune up, tune down) requesting the control logic to advance or to delay the clock management circuit phase by one step (or a small fixed number of steps) and an additional output (~~time~~ tune done) provided in response to "tune up" and "tune down" indicating that the requested operation has been completed. Advancing or delaying the clock management circuit phase by one step or a small fixed number of steps allows to smooth sampling clock phase variations without the need of additional circuitry: it acts as an built-in integrator.

Kindly amend paragraph [0019] of the specification as follows:

[0019] At the same time that "aligned" line is asserted, the initial number of steps used to cancel the phase shift in clock phase alignment 30 is stored in a first register 40. Likewise, when the output line "aligned" 42 of clock phase alignment circuit 38 is asserted, the initial number of steps used to cancel the phase shift in this circuit is stored in a second register 44. Then, at each subsequent phase alignment operation, the number of steps which have been necessary to cancel the phase shift are subtracted in subtractor 46 for clock phase alignment circuit ~~38~~ 30 and in subtractor 48 for clock phase alignment circuit 38 in order to know the deviation value for each circuit. Then, the phase control logic 50 which is typically a state machine performs a comparison between deviations provided by

the first and the second clock phase alignment circuitry 30 and 38 in order to forward either a tune up signal or a tune down signal on lines 52 to the first clock phase alignment circuit 30 in order to control this one in the operation of canceling the phase shift. Note that the phase control logic 50 provides also a reset signal on line 54 to the clock phase alignment circuit 38, and the reset releasing signal on the same line to launch the phase shift operation by the clock phase alignment circuit 38.